REMARKS

Status of Claims

Claims 20-52 of the present application have been withdrawn due to the July 29, 2005 Restriction Requirement.

Claims 1-19 are currently pending for examination, of which claims 1, 12, and 13 have been amended to further delineate the claimed invention of the present application.

Specifically, claim 1 has been amended to further recite that the dielectric cap of each polySi gate "comprises a first dielectric material," that the dielectric stack "comprises a first, lower dielectric layer and a second, upper dielectric layer, wherein the first, lower dielectric layer comprises the first dielectric material, and wherein the second, upper dielectric layer comprises a second, different dielectric material," that planarization of the dielectric stack "remove[s] an upper portion of the second, upper dielectric layer," and that the etching process "selectively remove[s] the first, lower dielectric layer and the dielectric cap against the second, upper dielectric layer to thereby expose only an upper surface of each polySi gate, wherein the exposed upper surface of each polySi gate is below an upper surface of the second, upper dielectric layer." Support for such claim amendments can be found in the instant specification at paragraphs [0077], [0078], [0080], and [0081] and Figures 4-6. Figure 6 specifically shows that after the etching process, only the upper surface (not the sidewalls) of each polySi gate 16 is exposed, and the exposed upper surface of polySi gate 16 is below the upper surface of the second dielectric layer 32.

Claim 12 has been amended to recite that "the first dielectric material is a nitride, and wherein the second dielectric material is an oxide." Support for such a claim amendment can be found in paragraph [0077] and [0078] of the instant specification.

Claim 13 has been amended to recite that "the step of planarizing comprises chemical mechanical polishing." Support for such a claim amendment can be found in paragraph [0080] of the instant specification.

Therefore, amendments of claims 1, 12, and 13 introduce no new matter.

Response to the §103 Rejections

In the September 9, 2005 Office Action, the Examiner rejected claims 1-19 under 35 U.S.C. §103(a) on various reference grounds. Specifically, the Examiner rejected:

- Claims 1-5, 7-9, 12 and 14-19 as alleged obvious over U.S. Patent No. 6,867,130 to Karlsson et al. (hereinafter "Karlsson") in view of U.S. Patent No. 5,153,485 to Pey et al. (hereinafter "Pey");
- Claim 6 as alleged obvious over Karlsson in view of Pey and further in view of U.S. Patent No. 6,596,576 to Fu et al. (hereinafter "Fu");
- Claim 11 as alleged obvious over Karlsson in view of Pey and further in view of U.S. Patent No. 6,100,145 to Kepler et al. (hereinafter "Kepler"), and
- Claim 13 as alleged obvious over Karlsson in view of Pey and further in view of U.S. Patent No. 6,924,184 to Cave et al. (hereinafter "Cave").

Applicants respectfully traverse the §103 rejections of claims 1-19, as amended herein, for the following reasons:

The amended claim 1, from which claims 2-19 depend, positively recites a dielectric cap that is located on an upper surface of each polySi gate and comprises a first dielectric material, and a dielectric stack that comprises a first, lower dielectric layer and a second, upper dielectric layer, wherein the first, lower dielectric layer comprises the first dielectric material, and wherein the second, upper dielectric layer comprises a second, different dielectric material. More importantly, the amended claim 1 recites planarization of the dielectric stack to remove an upper portion of the second, upper dielectric layer, followed by an etching process to selectively remove the first, lower dielectric layer and the dielectric cap against the second, upper dielectric layer to thereby expose *only* an upper surface of each polySi gate, wherein the exposed upper surface of each polySi gate is *below* an upper surface of the second, upper dielectric layer, as shown in Figure 6 of the instant specification.

None of the references cited by the Examiner discloses an etching process that selectively removes a first dielectric layer and a dielectric cap against a second dielectric layer to thereby expose only an upper surface of a polySi gate and resulting in an exposed upper surface of the polySi gate that is below an upper surface of the second dielectric layer, as positively recited by claim 1 of the present application.

The Karlsson reference does not disclose any dielectric cap (as expressly conceded by the Examiner in the September 9, 2005 Office Action). Further, Karlsson discloses only one dielectric layer 20, and it does not provide any derivative basis for an etching process that selectively removes a first dielectric layer and a dielectric cap against a second dielectric layer.

Moreover, the only dielectric layer 20 disclosed by Karlsson is etched back to expose not only an upper surface of the gate electrodes 12 (which contains the metal silicide layers 17), but also the upper sidewalls of the gate electrodes 12, and the upper surface of each gate electrode 12

is above, instead of below, the upper surface o the etched-back dielectric layer 20, as clearly shown in Figure 3 of Karlsson.

The Pey reference discloses only one dielectric layer 28 (also referred to as 28A and 28B), so it does not provide any derivative basis for an etching process that selectively removes a first dielectric layer and a dielectric cap against a second dielectric layer.

Further, the only dielectric layer 28 disclosed by Pey is first planarized (as 28A in Figure 2 of Pey) and then etched back (as 28B in Figures 3A and 3B of Pey) to a level below the upper surfaces of the gate electrodes 16 and 18. The subsequent etching of the dielectric cap 20, as disclosed by Pey, not only exposes the upper surfaces of the gate electrodes 16 and 18, but also the upper sidewalls of the gate electrodes 16 and 18 (as shown in Figures 4A and 4B of Pey). Therefore, the upper surfaces of the gate electrodes 16 and 18 are above, instead of below, the upper surface of the etched-back dielectric layer 28B, as clearly shown in Figures 4A and 4B of Pey.

The Fu reference was cited by the Examiner for its disclosure of a first and second spacer. Therefore, the applied disclosure of Fu cannot remedy the deficiency of Karlsson and Pey.

The Kepler reference was cited by the Examiner for its disclosure of formation of a silicon layer atop the semiconductor substrate prior to metal deposition. Therefore, the applied disclosure of Kepler cannot remedy the deficiency of Karlsson and Pey.

Cave discloses a dielectric stack that comprises a first dielectric layer 32 formed of nitride and a second dielectric layer 34 formed of a phosphorous doped silicon glass (see Cave, column 3, lines 32-37), followed by chemical mechanical polishing to form coplanar surfaces of the first and second dielectric layers 32 and 34 (column 4, lines 8-10, Figure 3).

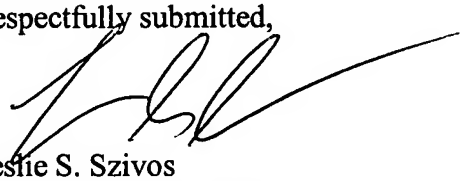
However, nothing in Cave teaches or suggests an etching process that selectively removes the first dielectric layer against the second dielectric layer. On the contrary, a non-selectively etching process is used by Cave to etch through both layers 32 and 34 (see Cave, column 4, lines 60-61, and Figure 6).

Therefore, like Karlsson and Pey, Cave fails to provide any derivative basis for an etching process that selectively removes a first dielectric layer and a dielectric cap against a second dielectric layer.

It is therefore clear that claims 1-19 patentably distinguish over all the cited references, by positively reciting an etching process that selectively removes a first dielectric layer and a dielectric cap against a second dielectric layer, to thereby expose only an upper surface of a polySi gate and resulting in an exposed upper surface of the polySi gate that is below an upper surface of the second dielectric layer.

Based on the foregoing, favorable reconsideration and allowance of the amended claims 1-19 of the present application are respectfully requested.

Respectfully submitted,



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